OVERVIEW

The CF5008A1 is a VCXO module IC that employs a circuit structure with low parasitic capacitance effects and a wide frequency range. Built-in components mean that few external components are required to construct a VCXO.

FEATURES

- Up to 30 MHz operation
- Inverter amplifier feedback resistor built-in
- 8 mA (V_{DD} = 5 V), 4 mA (V_{DD} = 3 V) drive capability
- 2.7 to 5.5 V supply voltage
- Circuit structure with low parasitic capacitance effects
  - Direct connection to varicap diodes and crystal
- Few external components required to form a VCXO
- Amplitude limiting resistor Rd built-in
- Chip form (CF5008A1)

SERIES CONFIGURATION

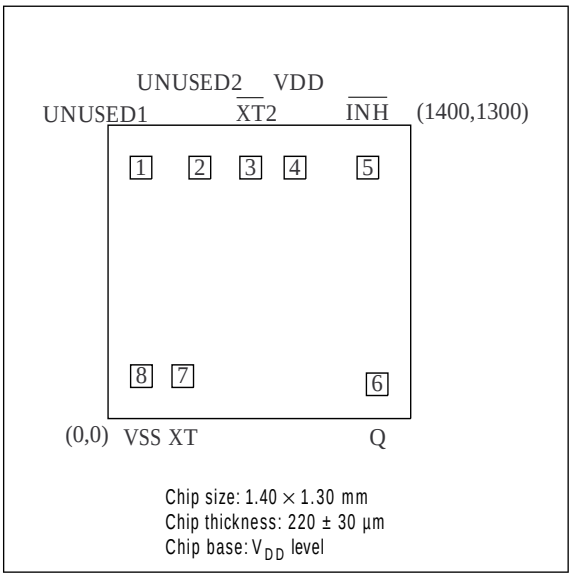
Version	Output frequency	Input level	Output duty level	Standby output state
CF5008A1	f_O	CMOS	CMOS	High impedance

ORDERING INFORMATION

Device	Package
CF5008A1–2	Chip form

PAD LAYOUT

(Unit : µm)

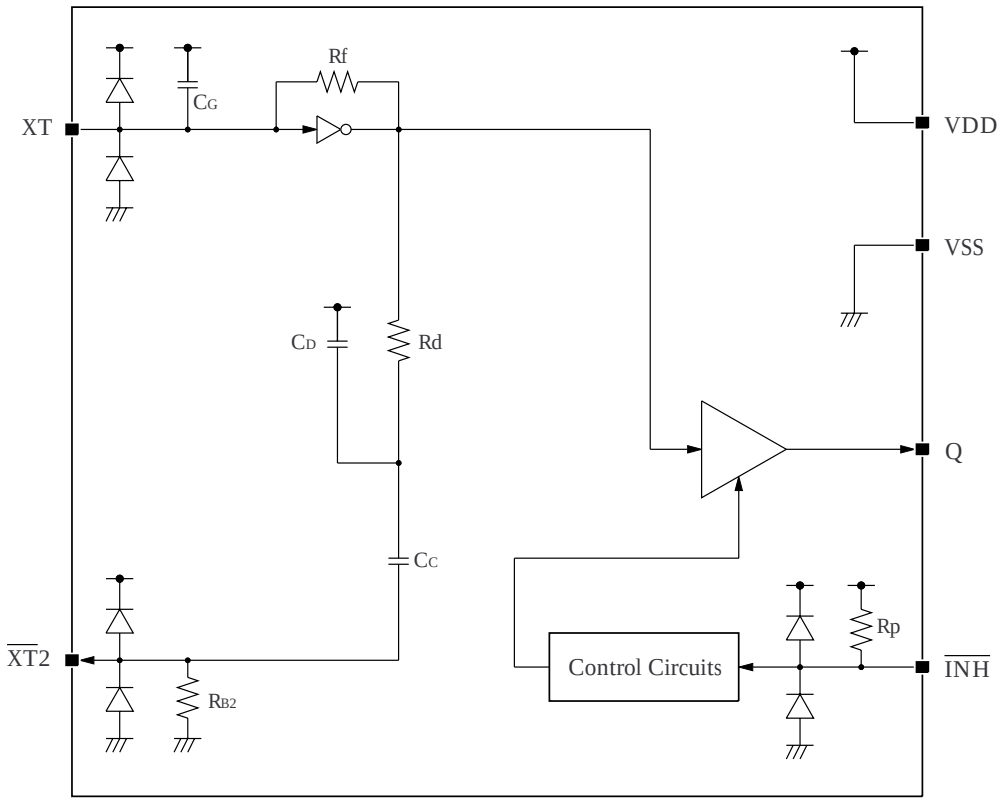


Chip size: 1.40 × 1.30 mm
Chip thickness: 220 ± 30 µm
Chip base: V_{DD} level

PAD DIMENSIONS

Number	Name	I/O	Description	Pad dimensions [µm]	
				X	Y
1	UNUSED1	–	Not used.	153	1112
2	UNUSED2	–	Not used.	425	1112
3	$\overline{XT}$2	O	Oscillator output pin	660	1112
4	VDD	–	Supply voltage	865	1112
5	$\overline{INH}$	I	Output-control input pin. Q signal output enabled when HIGH or open. High-impedance output when LOW.	1202	1112
6	Q	O	Output pin	1245	152
7	XT	I	Oscillator input pin	346	188
8	VSS	–	Ground	155	188

BLOCK DIAGRAM



OSCILLATOR ELEMENT CONSTANTS (typical values)

	R_{B1}	R_{B2}	R_d	R_f	R_p	C_G	C_D	C_C
CF5008A1	100kΩ	50kΩ	450Ω	150kΩ	100kΩ	20pF	10pF	70pF

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.5 to 7.0	V
Input voltage range	V_{IN}		–0.5 to V_{DD} + 0.5	V
Output voltage range	V_{OUT}		–0.5 to V_{DD} + 0.5	V
Operating temperature range	T_{opr}		–40 to 85	°C
Storage temperature range	T_{stg}		–65 to 150	°C
Output current	I_{OUT}		25	mA

Recommended Operating Conditions

V_{SS} = 0 V, CL ≤ 15 pF, f ≤ 32.5 MHz

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.7	–	5.5	V
Input voltage	V_{IN}		V_{SS}	–	V_{DD}	V
Operating temperature	T_{OPR}		–20	–	80	°C

Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 80 °C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, I_{OH} = 8 mA, V_{DD} = 4.5 V	4.0	4.2	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 1, I_{OL} = 8 mA, V_{DD} = 4.5 V	–	0.3	0.4	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH}$ = LOW, V_{OH} = V_{DD}	–	–	10	µA
		Q: Measurement cct 2, $\overline{INH}$ = LOW, V_{OL} = V_{SS}	–	–	10	
HIGH-level input voltage	V_{IH}	$\overline{INH}$	0.8V_{DD}	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$	–	–	0.2V_{DD}	V
Current consumption	I_{DD}	$\overline{INH}$ = open, Measurement cct 3, load cct 1, C_L = 15 pF, f = 30 MHz	–	28	65	mA
$\overline{INH}$ pull-up resistance	R_{UP}	Measurement cct 4	50	–	150	kΩ
Feedback resistance	R_f	Design value, determined by the internal wafer pattern	–	150	–	kΩ
Built-in resistance	R_d	Design value, determined by the internal wafer pattern	–	450	–	Ω
	R_c		–	0	–	Ω
	R_{B1}	Measurement cct 5	–	100	–	kΩ
	R_{B2}	Measurement cct 6	–	50	–	kΩ
Built-in capacitance	C_G	Design value, determined by the internal wafer pattern	–	20	–	pF
	C_D		–	10	–	pF
	C_C		–	70	–	pF

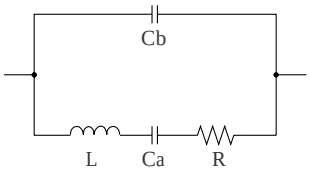
Switching Characteristics

V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 80 °C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 3, load cct 1, 0.1V_{DD} to 0.9V_{DD}, C_L = 15 pF	V_{DD} = 2.7 to 3.6 V	–	3	8	ns
			V_{DD} = 4.5 to 5.5 V	–	2.5	6	
Output fall time	t_{f1}	Measurement cct 3, load cct 1, 0.9V_{DD} to 0.1V_{DD}, C_L = 15 pF	V_{DD} = 2.7 to 3.6 V	–	3	8	ns
			V_{DD} = 4.5 to 5.5 V	–	2.5	6	
Output duty cycle[1]	Duty	Measurement cct 3, load cct 1, Ta = 25 °C, C_L = 15 pF, f = 32MHz	V_{DD} = 3.0 V	42	–	58	%
			V_{DD} = 5.0 V	42	–	58	
Output disable delay time	t_{PLZ}	Measurement cct 7, load cct 1, Ta = 25 °C, $C_L \leq$ 15 pF		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

1. Determined by the lot monitor.

Current consumption and Output waveform with NPC's standard crystal



f (MHz)	R (Ω)	L (mH)	Ca (fF)	Cb (pF)
30	17.2	4.36	6.46	2.26

FUNCTIONAL DESCRIPTION

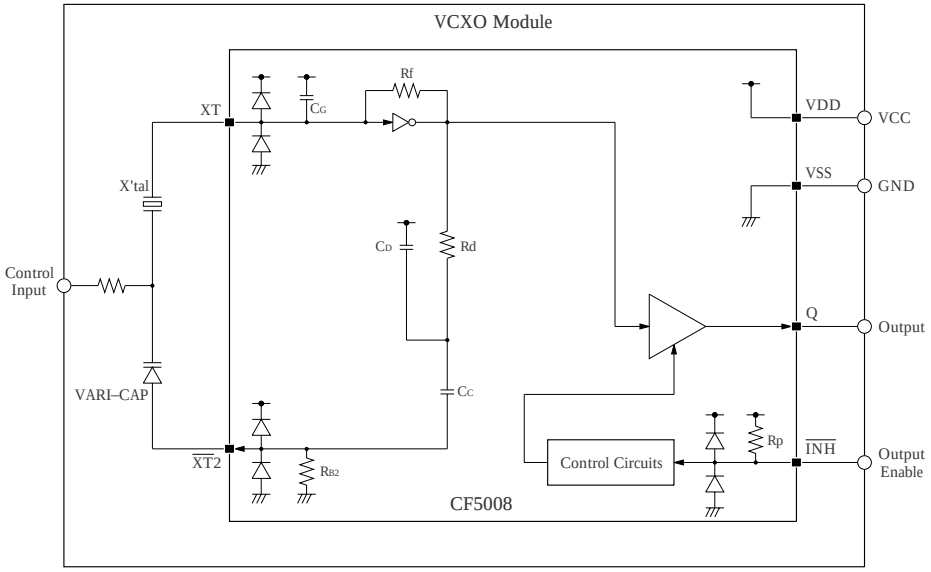
Standby Function

The oscillator output on Q changes as shown in the following table when $\overline{INH}$ goes LOW.

$\overline{INH}$	Q	Oscillator
HIGH (or open)	f_O	Normal operation
LOW	High impedance	Normal operation

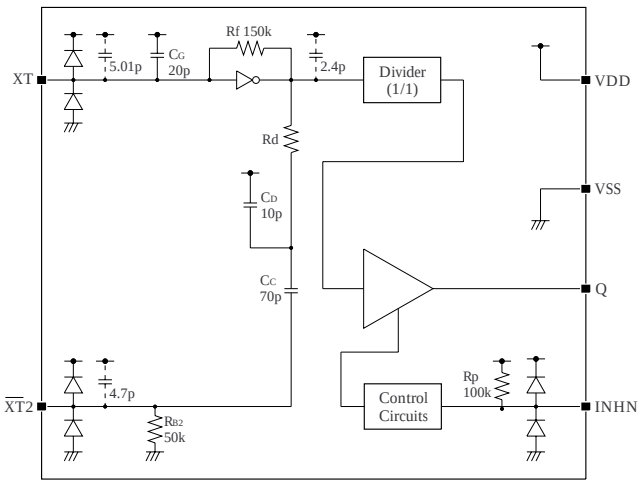
TYPICAL APPLICATION CIRCUIT

Typical circuit structures (C_G and C_D) that use a varicap device have a reduced frequency range due to the effects of parasitic capacitance. The CF5008A1, however, has built-in components C_C and R_{B2} that are connected in series with the varicap device, increasing the frequency output range.



PARASITIC CAPACITANCE

Parasitic capacitance are unwanted capacitance effects that occur due to the junction capacitance where the protection diodes and transistor drains are connected to the substrate. The following equivalent circuit figure shows the calculated parasitic capacitances. The surface area for each component is calculated from the IC layout pattern, and the capacitance calculated per unit area.



VARICAP (Variable Capacitance Diodes) SELECTION

The CF5008A1 forms a VCXO with addition of an external varicap (variable capacitance diode) device. This section examines the results using various varicap devices. When the equivalent circuit in figure 1 is used, the load capacitance C_L must be changed by a factor of 4 to 5 (10 to 40pF) to affect a ±100ppm frequency change. Varicap devices that can change the capacitance by a factor of 5 require a maximum capacitance in the range approximately 20 to 50pF. Devices matching this criteria are listed in the following table.

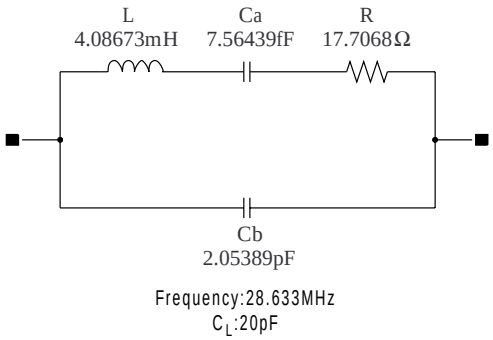
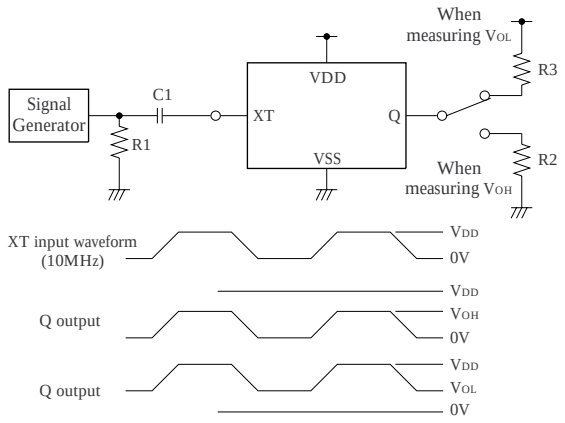


Figure 1. Crystal oscillator element equivalent circuit

Company	Product	Capacitance 1	Capacitance 2
HITACHI	HVU17	50.0 to 85.0pF (VR = 1V)	5.23 to 8.84pF (VR = 4.5V)
HITACHI	HVU359	24.8 to 29.8pF (VR = 1V)	6.00 to 8.30pF (VR = 4V)
HITACHI	HVU362	41.6 to 49.9pF (VR = 1V)	10.1 to 14.8pF (VR = 4V)
HITACHI	HVC374B	21.5 to 24.0pF (VR = 1V)	12.5 to 14.5pF (VR = 2V)
HITACHI	HVC375B	15.5 to 17.0pF (VR = 1V)	4.0pF typ (VR = 4V)
Panasonic	MA304	24.8 to 29.8pF (VR = 1V)	6.00 to 8.30pF (VR = 4V)
Panasonic	MA2S304	24.8 to 29.8pF (VR = 1V)	6.00 to 8.30pF (VR = 4V)
Panasonic	MA2ZV05	18.5 to 20.5pF (VR = 1V)	3.60 to 4.10pF (VR = 4V)
TOKO	KV1811E	21.5pF typ (VR = 1V)	4.00pF typ (VR = 4V)
TOKO	KV1812	16.0pF typ (VR = 1V)	3.00pF typ (VR = 4V)

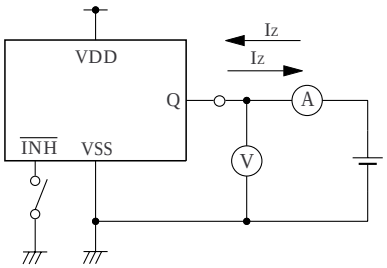
MEASUREMENT CIRCUITS

Measurement cct 1

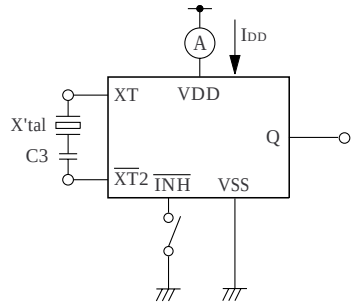


C1 : 0.001µF
R1 : 50Ω
R2 : 500Ω
R3 : 512.5Ω

Measurement cct 2

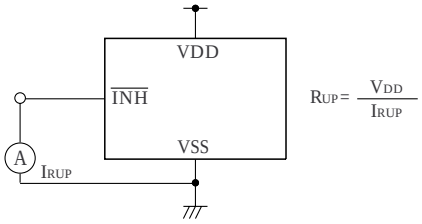


Measurement cct 3

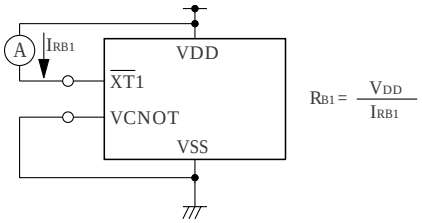


C3 : 15pF

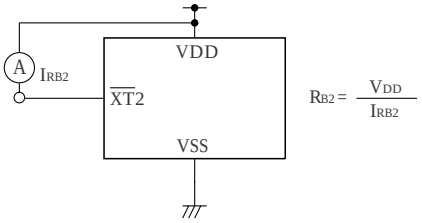
Measurement cct 4



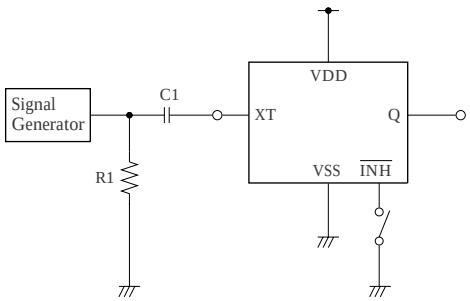
Measurement cct 5



Measurement cct 6

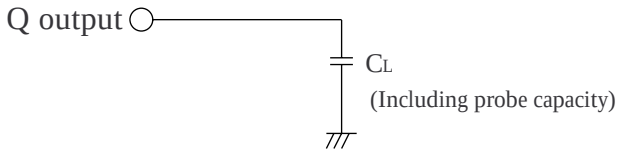


Measurement cct 7



C1 : 0.001µF
R1 : 50Ω

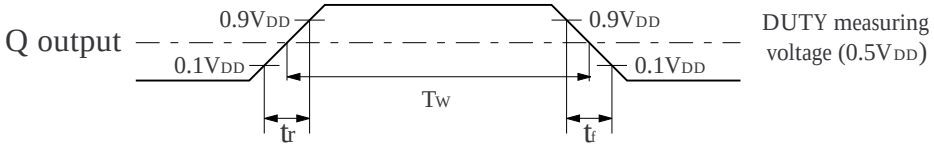
Load cct 1



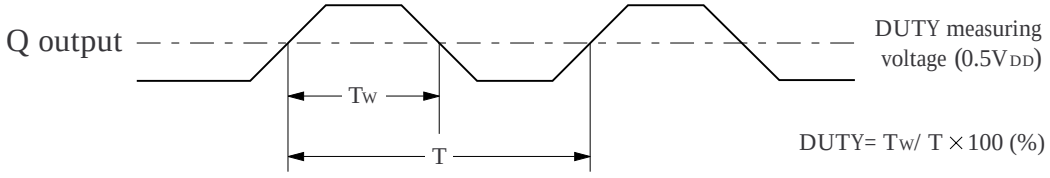
C_L = 15pF : I_{DD} , DUTY, t_{f1} , t_{f1}

Switching Time Measurement Waveform

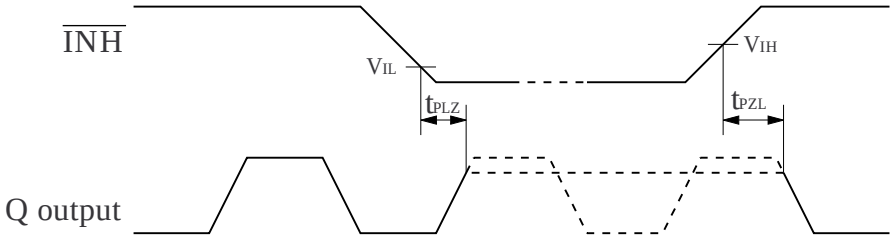
Output duty level (CMOS)



Output duty cycle (CMOS)



Output Enable/Disable Delay



$\overline{INH}$ inputwaveform tr = tf ≤10ns

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